Amendments to the Claims

IN THE CLAIMS:

Please amend claims 1-3 and 5 as follows:

1. (Currently Amended) A method of matching impedances across reducing impedance variations in an electrical circuit configured for placement on an integrated circuit (IC) including substrate, the electrical circuit including an electrical component having (i) input and output ports and (ii) a plurality of interconnected cascaded impedance devices configured for connection along a feedback path formed between the input and output ports, each impedance device having a predetermined an impedance value, the method comprising:

forming groups ~~sets~~ of ~~parallel connected~~ resistors, each group ~~set~~ (i) corresponding to one of the impedance devices, (ii) including two or more ~~parallel~~ resistor paths, and (iii) having a combined ~~total~~ impedance value substantially equal to the ~~predetermined~~ impedance value of its corresponding ~~impedance~~ device; and

configuring the groups ~~sets~~ of ~~parallel~~ resistor paths to form an interdigital structure across a ~~the~~ substrate when the IC ~~electrical circuit~~ is placed thereon, the interdigital structure being formed when the ~~parallel~~ resistor paths split at one point on the substrate and recombine at another point.

2. (Currently Amended) An apparatus for matching impedances across ~~reducing impedance variations in an electrical circuit structured and arranged for placement on~~ an integrated circuit (IC) including ~~substrate, the electrical circuit including an electrical component having (i) input and output ports and (ii)~~ a plurality of interconnected

~~cascaded~~ impedance devices ~~configured for connection along a feedback path formed between the input and output ports~~, each ~~impedance device~~ device having ~~a~~ ~~predetermined~~ an impedance value, the apparatus comprising:

means for forming groups ~~sets~~ of ~~parallel connected~~ resistors, each group ~~set~~ (i) corresponding to one of the impedance devices, (ii) including two or more parallel resistor paths, and (iii) having a combined ~~total~~ impedance value substantially equal to the ~~predetermined~~ impedance value of its corresponding ~~impedance~~ device; and

means for configuring the groups ~~sets~~ of parallel resistor paths to form an interdigital structure across a ~~the~~ substrate when the IC ~~electrical circuit~~ is placed thereon, the interdigital structure being formed when the parallel resistor paths split at one point on the substrate and recombine at another point.

3. (Currently Amended) The apparatus of claim 2, wherein the IC comprises ~~electrical component is~~ a programmable gain amplifier (PGA).

4. (Original) The apparatus of claim 3, wherein the PGA is a differential amplifier.

5. (Currently Amended) The apparatus of claim 4, wherein the ~~predetermined~~ impedance values of all of the impedance devices are substantially equal.

6. (Original) The apparatus of claim 5, wherein the IC is formed in CMOS.